Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	10/630,480	AVERBUJ ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2117	

All Participants:

(1) *Cynthia Britt*.

(2) *Kenyon S. Jenckes, Reg. No. 41,873*.

Status of Application: _____

(3) _____.

(4) _____.

Date of Interview: *31 August 2007*

Time: *2PM*

Type of Interview:
- ☒ Telephonic
- ☐ Video Conference
- ☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☒ No
If Yes, provide a brief description:

Part I.

Rejection(s) discussed:
N/A

Claims discussed:
Claims 1, 26, 28

Prior art documents discussed:
N/A

Part II.

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:
See Continuation Sheet

Part III.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.

☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

CYNTHIA BRITT
PRIMARY EXAMINER
Cynthia Britt 8.31.07
(Examiner/SPE Signature)

(Applicant/Applicant's Representative Signature – if appropriate)

Continuation of Substance of Interview including description of the general nature of what was discussed: Ways to clarify the claim language in order to place this application in condition for allowance were discussed and the following was agreed upon:

1. A system comprising:
a centralized built-in self-test (BIST) controller for testing a plurality of separate chips each containing one or more memory modules, wherein the BIST controller stores an the algorithm as a set of generalized commands that conform to a command protocol; and
a plurality of distributed sequencers that interpret the commands based on the command protocol and apply the generalized commands to the memory modules, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains.

26. A device comprising: a centralized built-in self-test (BIST) control means for issuing commands that conform to a generalized command protocol and define a BIST algorithm for testing a plurality of separate chips each containing one or more distributed memory modules having different timing requirements and physical characteristics; and distributed means for interpreting the commands and applying the commands to the memory modules in accordance with timing requirements and physical characteristics of the memory modules, said distributed means including a plurality of sequencers, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains.

28. A method comprising: applying an algorithm from a centralized built-in self-test (BIST) controller by issuing generalized commands that conform to a command protocol, to test a plurality of separate chips each containing one or more memory modules; and interpreting the commands with a distributed set of sequencers to apply the commands as one or more sequences of memory operations in accordance with the command protocol, each sequencer being associated with one or more memory modules operating on a common clock domain, wherein at least two of the sequencers are associated with memory modules operating on different clock domains.
It was agreed that the examiner would do an examiner's amendment in order to allow the application. However, it was discovered during an interference search that another US Patent issued to applicant claimed substantially the same invention. Therefore, the allowance of this application will not be made at this time. .